CLAIMS

What is claimed is:

1. A frequency monitor, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the resistive circuit; and

an indicator circuit which produces an output responsive to the charge held by the capacitor.

2. The frequency monitor of Claim 1, wherein the resistive circuit comprises:

a switched capacitor circuit which charges and discharges at a rate that depends on the rate of the edge detector output pulses.

3. The frequency monitor of Claim 1, wherein the indicator circuit comprises

a comparator that produces the indicator circuit output, said output being at one of two levels based on the charge and a threshold, a first level indicating that the difference between the two input signal frequencies is less than a predetermined amount, and the second level indicating that said difference is greater than a predetermined amount.

4. The frequency monitor of Claim 1, further comprising:

a selector which, responsive to the indicator circuit output, selects from plural sources to control an oscillator.

5. The frequency monitor of Claim 4, wherein the oscillator is a voltage-controlled oscillator.

6. The frequency monitor of Claim 4, wherein the plural sources are a data phase detector circuit and a frequency acquisition circuit.

7. The frequency monitor of Claim 6, wherein the oscillator produces a clock signal at a sampling frequency, the clock signal being used by the detector circuit to receive data.

8. The frequency monitor of Claim 7, wherein the frequency acquisition circuit compares the clock signal with a reference clock to produce a frequency acquisition output indicative of a difference between the frequencies of the reference clock and the oscillator clock signal, said output being one of the sources to the selector.

9. The frequency monitor of Claim 7, wherein the data phase detector circuit compares the clock signal with a rate of incoming data to produce a data phase detector output indicative of a difference between the frequencies of the reference clock and the incoming data, said output being one of the sources to the selector.

10. The frequency monitor of Claim 9, wherein the data phase detector circuit output comprises the error signal.

11. The frequency monitor of Claim 1, further comprising:

a combiner circuit which combines the two input signals to produce the error signal.

12. The frequency monitor of Claim 11, wherein the combiner circuit comprises:

a mixer which mixes the two input signals to produce a mixed signal; and

a low-pass filter which filters the mixed signal to produce the error signal.

13. A frequency lock system, comprising:

an oscillator which produces an output signal whose frequency is responsive to a control signal;

a frequency detector circuit which produces a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

a data recovery phase detector circuit which produces a phase detector output signal based on the oscillator output signal's frequency and an input stream's data frequency; and

a selector which selects either the frequency detector output signal or the phase detector output signal as the control signal.

14. The frequency lock system of Claim 13, further comprising:

a frequency monitor which controls the selector.

15. The frequency lock system of Claim 14, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and input data frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

16. The frequency lock system of Claim 14, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and a reference clock

frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

17. A method for monitoring frequency, comprising:

producing an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

charging a capacitor to a charge responsive to the error signal frequency; and

indicating, responsive to the charge held by the capacitor, a difference between the two input signal frequencies is less than a predetermined amount.

18. The method of Claim 17, further comprising:

using a switched capacitor circuit to charge the capacitor, the switched capacitor circuit having an effective resistance that depends on error signal frequency.

19. The method of Claim 17, further comprising:

selecting, responsive to the step of indicating, from plural sources to control an oscillator.

20. The method of Claim 19, wherein the oscillator is a voltage-controlled oscillator.

21. The method of Claim 19, wherein the plural sources are a data phase detector circuit and a frequency acquisition circuit.

22. The method of Claim 21, wherein the oscillator produces a clock signal at a sampling frequency, the clock signal being used by the detector circuit to receive data.

23. The method of Claim 22, wherein the frequency acquisition circuit compares the clock signal with a reference clock to produce a frequency acquisition output indicative of a difference between the frequencies of the reference clock and the oscillator clock signal, said output being one of the sources to the selector.

24. The method of Claim 22, wherein the data phase detector circuit compares the clock signal with a rate of incoming data to produce a data phase detector output indicative of a difference between the frequencies of the reference clock and the incoming data, said output being one of the sources to the selector.

25. The method of Claim 24, wherein the data phase detector circuit output comprises the error signal.

26. The method of Claim 17, further comprising:

combining the two input signals to produce the error signal.

27. The method of Claim 26, wherein the step of combining comprises:

mixing the two input signals to produce a mixed signal; and

filtering, with a low-pass filter, the mixed signal to produce the error signal.

28. A frequency lock method, comprising:

producing, from an oscillator, an output signal whose frequency is responsive to a control signal;

producing, from a frequency detector circuit, a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

producing, from a data recovery phase detector circuit, a phase detector output signal based on the oscillator output signal's frequency and an input stream's data frequency; and

selecting either the frequency detector output signal or the phase detector output signal as the control signal.

29. The method of Claim 28, further comprising:

controlling the selector with a frequency monitor.

30. The method of Claim 29, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and input data frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

31. The method of Claim 29, wherein the frequency monitor selects the phase detector output signal if the oscillator frequency and a reference clock frequency are within a predetermined margin, and selects the frequency detector output signal otherwise.

32. A frequency monitor, comprising:

means for producing an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

means for charging a capacitor to a charge responsive to the error signal frequency; and

means for indicating, responsive to the charge held by the capacitor, whether the difference between the two input signal frequencies is less than a predetermined amount.

33. The frequency monitor of Claim 32, further comprising:

means for selecting, responsive to the step of indicating, from plural sources to control an oscillator.

34. The frequency monitor of Claim 32, further comprising:

means for combining the two input signals to produce the error signal.

35. A frequency lock system, comprising:

means for producing, from an oscillator, an output signal whose frequency is responsive to a control signal;

means for producing, from a frequency detector circuit, a frequency detector output signal based on the oscillator output signal's frequency and a reference clock frequency;

means for producing, from a data recovery phase detector circuit, a phase detector output signal based on the oscillator output signal's frequency and an input stream's data frequency; and

means for selecting either the frequency detector output signal or the phase detector output signal as the control signal.